Claim Amendments:

Please amend the claims as indicated:

Claims 1-5 (Previously Cancelled)

6. (Currently Amended) A method of fabricating a semiconductor transistor comprising the steps of:

providing a gate structure having a sidewall portion and a top portion, said gate structure formed on a substrate;

forming a dielectric spacer formed over the substrate, said dielectric spacer forming an L-shape comprising a vertical portion parallel to the sidewall portion, and a horizontal portion approximately orthogonal to the sidewall portion of the gate structure;

forming a first source/drain region in the substrate during a source/drain implant using an implant species ~~selected from the group~~ of indium ~~and antimony~~, wherein the first source/drain region formed underneath the horizontal portion of the L-shaped dielectric spacer; and

forming a second source/drain region in the substrate during the source/drain implant using the implant species, wherein the second source/drain region is immediately adjacent the first source/drain region and has a depth greater than a depth of the first source/drain region.

7. (Previously Amended) The method of claim 6, further including a step of forming a liner oxide over said gate structure prior to the step of forming the dielectric spacer.

8. (Previously Cancelled)

9. (Cancel)

10. (Previously Cancelled)

11. (Cancel)

12. (Previously Amended) The method of claim 6 wherein said L-shaped dielectric spacer is a nitride.

13. (Previously Amended) The method of claim 6 wherein the length of the horizontal portion of the L-shaped dielectric spacer ranges from about 200 Angstroms to about 500 angstroms.

14. (Currently Amended) A method of fabricating a semiconductor transistor comprising the steps of:

forming a source/drain extension having an average extension depth

forming a first portion of a source/drain region underlying a horizontal midpoint location of a sidewall spacer of the semiconductor transistor, the first portion of the source/drain region having a first average depth and a first length; and

forming a second portion of the source/drain region simultaneously in time with the first portion, wherein the second portion has a second average depth and a second length, wherein the second average depth is greater than the first average depth, and the first average depth is greater than the average extension depth.

15. (New) The method of claim 14, wherein forming the first portion further comprises the horizontal midpoint location being at a horizontal portion of an L-shaped sidewall spacer, the horizontal portion being approximately orthogonal a sidewall portion of a gate of the semiconductor transistor.

16. (New) The method of claim 14, wherein the first length is substantially equal to a length of the horizontal portion of the L-shaped sidewall spacer.

17. (New) A method of fabricating a semiconductor transistor comprising the steps of:

providing a gate structure having a sidewall portion and a top portion, said gate structure formed overlying a substrate;

forming a dielectric spacer formed overlying the substrate, said dielectric spacer forming an L-shape comprising a vertical portion parallel to the sidewall portion, and a horizontal portion approximately orthogonal to the sidewall portion of the gate structure;

forming a first source/drain region in the substrate during a source/drain implant, wherein the first source/drain region is formed by implanting a dopant through the horizontal portion of the L-shaped dielectric spacer; and

forming a second source/drain region in the substrate during the source/drain implant using the implant species, wherein the second source/drain region is immediately adjacent the first source/drain region and has a depth greater than a depth of the first source/drain region, wherein forming the second source/drain and the first source/drain occurs simultaneously.

18. (New) The method of claim 14, wherein

forming the first portion comprises implanting a dopant in the first portion through the sidewall spacer; and

forming the second portion comprises implanting the dopant in the second portion simultaneously with implanting the dopant in the first portion.